STAND-ALONE/PARALLEL INTERFACE PRODUCTS

Using the Device

CHIP ENABLE INITIATED RECORD AND PLAYBACK CYCLES (ISD1000A, ISD2500)

The ISD data sheets describe a $\overline{CE}$ initiated Record and playback cycle. The designer sets the PD pin LOW to power up the device, sets up the address and P/$\overline{R}$ pins, waits T_{PUD}, and then drops $\overline{CE}$. The device then operates as desired. Once $\overline{CE}$ has fallen, the device ignores further transitions on the address and P/$\overline{R}$ pins. When PD has been LOW more than T_{PUD} before address and P/$\overline{R}$ pins are changed, these pins must be stable T_{SET} time before $\overline{CE}$ falls (T_{SET} is always very much shorter than T_{PUD}).

RECORD

$\overline{CE}$ controls start and stop of a Record cycle. The falling edge of $\overline{CE}$ starts Record and the rising edge stops Record within 12.5 to 37.5 msec. This time is utilized by the chip to complete programming cycles that may be under way.

PLAYBACK

A momentary LOW $\overline{CE}$ (at least T_{CE} long) initiates a playback cycle. After a playback cycle initiated by a momentary $\overline{CE}$ has been started, it will end one of three possible ways:

- The device reads an internal end of message (EOM) bit set HIGH. At this time, a T_{EOM} long $\overline{EOM}$ signal will be output while audio continues to be played out of the device. At the end of the $\overline{EOM}$ pulse, the audio output will cease.
- The device goes into the overflow condition (this assumes that an Operational Mode action is not under way; Operational Mode use of $\overline{EOM}$ will be covered later). $\overline{EOM}$ will go LOW and remain in that state. Audio output will continue for an additional T_{EOM} after $\overline{EOM}$ goes LOW. This means that the $\overline{EOM}$ signal actually goes LOW T_{EOM} before the device finishes playing its memory.
- A long Power-Down cycle is performed. If PD is held HIGH for at least T_{PUD} the playback cycle will be interrupted.

PD INITIATED RECORD AND PLAYBACK CYCLES (ISD1000A, ISD2500)

A Record or Playback cycle may be initiated by a falling PD. Address and P/$\overline{R}$ pins should be set up as desired and $\overline{CE}$ held LOW. When PD is changed to a LOW, the appropriate cycle will begin T_{PUD} after PD falls.

In this case, initially, the device will be powered down. When the PD pin is taken LOW, the device will "wake up" (i.e., come out of the Power-Down condition), read the current address and control pins, then execute the desired operation.

RECORD AND PLAYBACK CYCLES IN THE ISD1100/1200/1400 SERIES

The ISD1100/1200/1400 have a different interface than the ISD1000A and ISD2500. These devices do not have a PD pin. Power-down is always automatic. They also do not have $\overline{CE}$ or P/$\overline{R}$ pins. All operations start by changing state on a single input pin.

The ISD1100/1200/1400 interface consists of the following input pins: $\overline{REC}$, $\overline{PLAYE}$, $\overline{PLAYL}$. The only digital output is called $\overline{RECLED}$. Record is accomplished by holding the $\overline{REC}$ pin LOW for the duration of the Record. $\overline{RECLED}$ stays LOW during Record. Playback is started with a pulse on the $\overline{PLAYE}$ or "play edge" pin and will end with Automatic Power-Down when a set $\overline{EOM}$ or overflow is reached. $\overline{RECLED}$ pulses LOW momentarily at the end of the message. This pulse is an $\overline{EOM}$ pulse. The $\overline{PLAYL}$ or "play level" pin must be held LOW for the duration of the Playback. If it is taken back HIGH, Playback ceases. A $\overline{PLAYL}$ initiated Playback cycle will stop and Power-Down when a set EOM or overflow is reached even when the input is held LOW. Power-down is always automatic, regardless of how the Record or Playback cycle is ended.

The ISD1100 series has built in pull-up resistors on all three control inputs ($\overline{PLAYL}$, $\overline{PLAYE}$, and $\overline{REC}$). The presence of these on-chip resistors enables simple push buttons to control each input without other external components.

The ISD1100 series also has pull-up resistors on address lines A6 and A7 and pull-down resistors on A0 through A5. A Record or Playback Operation that begins with the address pins set in this manner will proceed exactly as if the device was addressed at address 0 with no Operational Mode set.

Additionally, the XCLK pin of the ISD1100 also has a pull-down resistor.

Care should be taken when using an ISD1100 series device in extremely LOW power applications. The input pins should not be continuously held "opposite" the associated on-chip resistor. Each pin with a pull-up or pull-down resistor has the potential for drawing approximately 50 μAmps of current when held at other than the correct supply voltage. For instance, if A6 and A7 were connected to V_{SS} in a circuit using an ISD1110, approximately 100 μAmps would be continuously dissipated. This current would be dissipated even when the device is powered down. The ISD1200 and ISD1400 devices do not have these pull-up or pull-down resistors.

CASCADING MULTIPLE DEVICES (ISD1000A, ISD2500)

Devices from several of the ISD device families may be cascaded together to enable the designer to achieve longer record and playback times. Both the ISD1000A series and the ISD2500 series have internal logic to enable the designer to easily cascade multiple devices. There is less than two microseconds of dropout when changing from device to device.

CASCADING THE ISD2500 SERIES

A complete cascading application for the ISD2500 series with a detailed explanation of its operation is included in the circuit example section that follows. There is also an explanation in the "Operational Modes" section under Application Information.

NOTE *The ISD2500 series includes additional logic to enable additional cascading features not provided in the ISD1000A series. This is covered in detail in the "Device Operation" under Application Information.*

CASCADING THE ISD1000A SERIES

In brief, the operation of $\overline{CE}$ and $\overline{EOM}$ during cascade operation proceeds as follows:

1. Set up the Operational Mode for cascade (A2, A5, A6 and A7 all HIGH).
2. A Record or Playback cycle is started with $\overline{CE}$.
3. When the first device in the cascade goes into overflow to indicate it is at memory end, the $\overline{EOM}$ pin goes LOW to provide a $\overline{CE}$ signal to the next device in the cascade.
4. Following devices are enabled in the same manner down the line.

Audio processing in the cascade mode may be handled several different ways. The easiest application uses the first device's microphone preamplifier and it's ANA OUT output during record to drive the ANA IN pins of each device in the cascade circuit. During playback, the SP+ output is fed back to the preceding device's AUX input. The first device in the series is connected to a speaker and provides the audio output for the system. Other methods will be discussed in the applications section.

ADDRESSING ACROSS A MULTI-DEVICE BOUNDARY (ISD1000A, ISD2500)

Some users of the ISD analog storage devices may need more address space than provided in a single device. The following description discusses methods by which the ISD1000A series may be used to achieve additional storage space. A method of accomplishing this with the ISD2500 series is included in the "Circuit Examples" under Application Information.

ADDRESS ACROSS A MULTIDEVICE BOUNDARY USING THE ISD1000A SERIES

There are two ways to approach this application. The simpler solution occurs when any single message is short and it is possible to contain any given selection of messages within a single ISD1000A. In this case, each device is addressed individually and the short message to be played is selected as needed.

The more complicated application requires a message field that is totally independent of chip boundaries. The ISD1000A device combines two functions in the $\overline{EOM}$ output pin. These two functions are end-of-message indication and overflow. If the system using the ISD1000A can retain a time map of each word or phrase stored, it can arbitrate this signal and determine which condition is occurring. It is necessary to have a system time resolution of less than 25 ms to accomplish this. It may also be necessary to externally drive the ISD1000A device's clock to achieve proper time synchronization.

When the controlling logic or microprocessor determines that an overflow has occurred, it will immediately drop $\overline{CE}$ to the next ISD1000A so that the audio output can continue.

The Operational Mode used in the cascading application described in "Device Operation" cannot be used when addressing across a chip boundary. This is because Operational Mode and the addressing of individual messages do not coexist.

LOOPING CONSIDERATIONS

There are several applications that require continuous, or intermittent, looping of record or playback of audio sound effects, voice, etc. All ISD single-chip voice record/playback devices have the ability to perform this task either self-contained on-chip or with external logic. The circuit example section of this document includes several different applications that fit different requirements.

Two basic methods are used to loop record or playback ISD devices. The first method uses an Operational Mode to carry out the loop. Only a message that begins at address 000 (the beginning of the memory) and does not completely fill the memory may be looped this way with the ISD1000A devices. The memory may be completely full in the ISD1100/1200/1400 or ISD2500 series.

The second method uses external logic to create a looping condition. A signal from $\overline{EOM}$ or $\overline{RECLED}$ is used to pulse $\overline{CE}$ or $\overline{PLAYE}$ to start a new repetitive playback cycle.

LOOPING WITH A CONTINUOUS TONE

Some customers want looping to generate a continuous tone for an extended period of time. The ISD Applications group achieved this using the $\overline{CE}$ initiated looping method in an ISD1016A with moderate results. A perfect waveform match at the transition between the end of memory (indicated by the $\overline{EOM}$) and beginning of the next cycle through the loop is difficult to achieve. The worst case 25 ms $\overline{EOM}$ granularity defines the problem.

Intermittent looping may be achieved using a timer (such as an NE555) reset by the $\overline{EOM}$ output. Upon time-out, the timer executes a new $\overline{CE}$ or Power-Down cycle starting the playback over.

CONTINUOUS RECORD LOOPING (ISD1000A)

Another frequently requested application schematic is a continuously looping record. Several considerations must be kept in mind including the write wear out mechanism inherent in EEPROM memory cells. A discussion of this phenomenon is found under Write Endurance Considerations in this chapter. A second consideration is how important it is for the user to know exactly where the looping record ends. If the looping record always ends on memory overflow, then the application is simple. If an accurate replay of the "last N seconds" is required, stopping at a random time, then the circuit requirements are more complex.

A looping record application in an ISD1000A device uses the $\overline{EOM}$ signal to start a new $\overline{CE}$ Record cycle. Since $\overline{EOM}$ is the overflow indication during Record, this signal indicates the end of the memory space. It is time to start Record over at the beginning of the memory. If you choose to stop the loop and playback the memory at the EOM boundary, then the memory contains the last N seconds of recorded data according to which of the ISD devices were used in the application.

The more complex (and more general) requirement is that the Record loop end at a random time. If $\overline{CE}$ is taken HIGH during a looping Record cycle the internal address location of this event is not available to external logic. An EOM bit is written into the memory to indicate this location. The ISD devices do not include a mechanism to read out the memory location of this EOM. Also, the transition from Record to Playback resets the internal address counter to 000.

It is easy to determine the point where recording ended in the Record Loop Application. It will be marked with a set EOM bit. The message cueing Operational Mode may be used to find this location in a few milliseconds and playback may then begin at exactly where Recording ceased.

CONTINUOUS RECORD LOOPING (ISD1100/1200/1400 AND ISD2500)

The M3 Looping Operational Mode is available in the ISD1100/1200/1400 and ISD2500 series devices during Record as well as Playback. Continuous record looping is possible in those products using only Operational Mode input address strapping.

AUDIO DRIVE LEVELS AND IMPEDANCES

The ISD devices may be driven by an external source other than a microphone. The characteristics of the two inputs are shown in Table 1.

EXTERNAL COMPONENTS

The ISD products require only a few external components in most applications. A list of these components and comments follow:

BYPASS CAPACITORS

A playback only application typically does not need bypass capacitors. In fact, a playback only application in an ISD1000A or ISD2500 can operate with switches and a speaker and no other components. An ISD1100 playback only circuit only requires the chip, a push-button and the speaker (since the $\overline{PLAYE}$ pull-up resistor is contained on-chip). Several of the circuits in the "Circuit Example" section under Application Information.

A record and playback application should have low impedance high frequency bypass capacitors from each V_{CC} power supply pin to ground. A value of 0.1 μF is recommended. In addition, a

large capacitor for low frequency bypassing should be used to further decouple the power supply. A value of 10 to 100 μF should work adequately.

Table 1: Drive Levels and Impedances

	MIC (Pin 17)	ANA IN (Pin 20)
Input Impedance	≈10 KΩ	≈2.7 KΩ
Max. Drive Level	20 mV p-p	50 mV p-p
AGC Control	up to 20 dB	none

COUPLING CAPACITORS

An application that directly drives one of the input pins of the ISD device requires a coupling capacitor to DC isolate the input. The design issues of concern are the required voltage specification for the capacitor, capacitor leakage and capacitor value. The value of the capacitor is determined by the required frequency response and this is covered elsewhere in this document.

NOTE ISD does not recommend using tantalum capacitors in coupling capacitor applications.

RESISTORS

In a typical application, resistors are not used in any gain or level critical areas. A 10 percent tolerance is adequate for most applications.

POWER SUPPLY CONSIDERATIONS

Standard ISD devices are designed to operate from a single 4.5 to 6.5 volt power supply, except for the ISD33000 series, which operates from a single 2.7 to 3.3 volt power supply. This supply should have a low internal impedance and be noise free. These factors are especially critical during the recording process; any high frequency noise appearing at the V_{CCA} supply pin (pin 16) may be recorded into the device's memory array. For this reason, it is also important that the connections to the power supply be short, and have little series resistance or inductance. Additionally, some types of power supplies tend to contain noise that falls within the passband of the ISD device. For instance, aircraft power supplies operating from 400 cycle AC or switching power supplies may require additional DC filtering to ensure they are "quiet."

Playback only applications are not as critical and can stand a higher internal power supply source impedance without appreciable sound quality degradation.

BATTERY OPERATION

Batteries are often used to power ISD applications. All ISD product families now support operation from 4.5 to 6.5 volts, except for the ISD33000 series, which supports operation from 2.7 to 3.3 volts. Higher voltage sources must be regulated down to this range. A simple shunt zener diode regulated supply is adequate for the average application that does not require low power. In multichip situations the zener is inadequate and a three terminal regulator must be used.

The designer of any passively regulated battery source supply should keep in mind that the internal resistance of a battery increases rapidly as it approaches a discharged condition. If this impedance is not lowered by effective decoupling, record quality will degrade.

If reliable high quality record and playback are required from a battery source supply, the designer should use a higher voltage battery and an active regulation device such as a 5-volt three terminal regulator.

LOW POWER OPERATION

Many applications of the ISD devices need long-life low-power battery operation. The ISD1100/1200/1400 and ISD2500 Families have automatic power down options to help achieve this goal. If the ISD1000A series is used, the PD pin must be taken HIGH using external circuitry to gain the very low power standby state. By using any of the

above procedures, standby currents near the "shelf life" of many batteries may be achieved. The actual battery life, of course, depends on how often the device is operated.

RECORD/PLAYBACK NOISE CONSIDERATIONS

A number of factors influence the practicable signal-to-noise record performance of the ISD devices. The power supply sensitivity has already been covered. Proper PC board layout can effect a large improvement in signal-to-noise by keeping the noise generating parts of the circuit separated from the low level input pins. The pins with a noise sensitivity are MIC (pin 17), ANA IN (pin 20), AGC (pin 19), and MIC REF (pin 18). Additional information on PC board layout may be found in the "Single-Chip Board Layout Diagrams" under Application Information.

The principal noise source from the ISD devices is V_{CCD}, pin 28, and during a Record cycle only. The frequency distribution of this noise may be found in several regions. One source is centered around 80 Hz which is the repetition rate of the internally generated EEPROM programming power supply. Another source may be found between 30 MHz and 200 MHz in a number of discrete bands. An FCC recognized testing lab has done an evaluation of the radiation from an unshielded ISD1016A recording application. The results from that investigation show the emissions to be below the FCC Class B Radiation Limit for a computational device. The results are available from ISD upon request.

There is no substantial noise source during a playback cycle. However one will hear the inherent noise from the array. This is a very low level "hiss." When viewed on an oscilloscope, the amplitude will be about 10 mV p-p from either speaker lead to ground. Measured with an AC meter this noise will be less than 4 mV RMS. This is from a recording made with ANA IN, pin 20, connected to ground through a 0.1 μF capacitor.

One potential noise source during record or playback of ISD single-chip voice record/playback devices is voltage over- or under-shoot on signals connected to the address and control pins. Continuous or very short duration signals (for instance address transition "ringing") greater than 0.3 volt over V_{CC} or under V_{DD} may cause a considerable increase in recorded noise. Care should be taken to ensure signals on all pins are always within data sheet specifications (currently 0.3 volts over- or under-shoot).

LOW NOISE AND/OR HIGH-POWER OUTPUT APPLICATIONS

Some applications need extremely low noise record and playback. A good example of such a requirement is where the output of an ISD device is going to be amplified and used to drive a high power public address speaker system. One method of achieving an improved signal-to-noise ratio is to use the speaker outputs to drive an expander circuit such as found in the Philips/Signetics NE575 Low Voltage Compandor. Since the ISD device records using automatic gain control, the expander half of the NE575 may be used by itself to re-establish the dynamic range of the original recording and attenuate background noise. The results are impressive with virtually no detectable noise in the "dead time" between words and phrases. Other circuits similar to the Phillips chip can achieve comparable results.

Additionally, a circuit such as the NE575 or high-power amplifier stage should be driven differentially from the ISD device. When the speaker + (or –) output is used to drive the next stage in a single ended configuration, a transient is generated when the speaker outputs are pulled to ground during the Power-Down or a Record Operation. This transient results in a loud pop. If output is taken differentially, this transient is minimized because both pins are taken to ground together.

An example application using the NE575 expander driven differentially is found in the "Circuit Examples" under Application Information. An example of an amplified speaker output circuit may also be found on the next page.

MAKING IT SOUND LOUDER

Many applications for ISD devices use very small speakers, often less than two inches in diameter. The basic sampling system used by all ISD single-chip voice record/playback devices in itself supports a wide frequency response, only limited in low frequency by the value of the coupling capacitors in the microphone and ANA IN to ANA OUT circuits. Small speakers usually do not reproduce low frequencies well. The result is that a "full bandwidth" recording often does not sound very loud when played through such a speaker. Another way to look at this is that the low frequency components consume much of the output power of the ISD speaker driver. This power is not usable by a small speaker.

One method of recording "louder" signals that reproduce well through a small speaker is to limit the ISD device's low-end frequency response. This may easily be done by decreasing the size of the coupling capacitors used in the microphone circuit. The ISD1400 data sheet shows 0.1 μF capacitors connected to MIC and MIC REF. This value results in signals above 160 Hz being recorded without attenuation. A better choice for a small speaker system is to change these capacitors to 0.01 μF. This results in a low end pole of approximately 1500 HZ, sharply rolling off frequency response below this value.

The resulting recording will be made without the low frequencies that distort a small speaker. The relative "loudness" of the playback will be increased.

The circuit designer should try several values of capacitance to determine what is best for a specific application.

REALLY MAKING IT LOUDER

The on-chip speaker drivers present in all current ISD single chip voice record/playback devices have adequate power output for most applications. Some applications, however, need more speaker power than these chips provide. Fortunately, a number of manufacturers make single chip or single module speaker amplifiers that range from a few hundred milliwatts to 50 watts or more into an 8 Ω load.

Most of these speaker amplifier devices are supported by manufacturer's applications information that shows a single ended connection to the audio source. In the case of the ISD products, however, there are advantages to a balanced feed to the amplifier circuit. The potential pop resulting from a Power-Down cycle, for instance, may be avoided by driving the speaker amplifier from both SP+ and SP–. Fortunately, many of the available speaker driver products have an operational amplifier front end that includes a differential input.

The following two circuits demonstrate the general method that may be used to increase the speaker drive from ISD products.

NOTE *ISD customers are strongly encouraged to obtain the appropriate data sheet from the listed manufacturer to determine exact device specifications and the suitability of these devices in their specific application.*

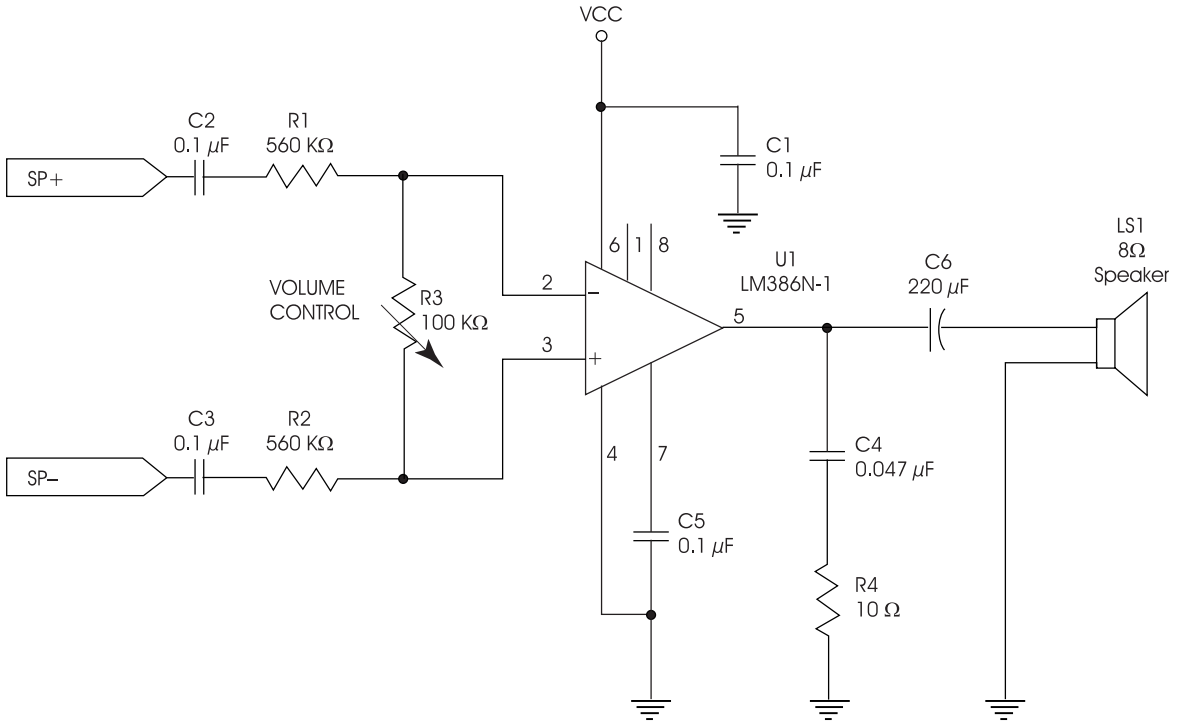
USING THE NATIONAL SEMICONDUCTOR CORPORATION LM386 LOW VOLTAGE AUDIO POWER AMPLIFIER

The NSC LM386 amplifier was designed for use in low voltage consumer applications. According to the NSC data sheet, it will operate over a voltage range of 4 to 12 volts or 5 to 18 volts. The voltage gain is adjustable from 20 to 200. At 6 volts the typical power output is 325 mW, at 9 volts it is 700 mW. (These numbers are at 10 percent THD.) In the circuit in Figure 1, the output level of the ISD device must be attenutated by resistors R1 and R2 before it can be applied to the inputs of the LM386. This is because the ISD device output leads are designed to drive a speaker directly to 12.5 mW. The voltage swing drives the LM386 into distortion if not reduced. At 5 volts, the value required is approximately 1 MΩ; at 9 volts the resistors can be at 560 KΩ. This is because the input pins of the LM386 have about a 50 KΩ to ground impedance, forming a voltage divider. Using 560 KΩ resistors and putting the 100 KΩ potentiometer R3 across the input pins creates a volume control.

The LM386 data sheet includes various applications circuits, all single ended. To eliminate the "pop" that can occur with the ISD speaker outputs being used single ended, the LM386 is used differentially. This lets the common mode rejection of the LM386 reduce the "pop" considerably. Because the differential connection is DC isolated, the LM386 can be run at any voltage in its allowable range while the ISD device remains at 5 volts. This give the designer some options as far as required power output for the particular application.

In the example circuit in Figure 1, pins 1 and 8 are left open for minimum gain of 20 in the LM386N-1. Then a volume control is provided in the potentiometer (R3) across pins 2 and 3.

Figure 1: LM386 Speaker Driver

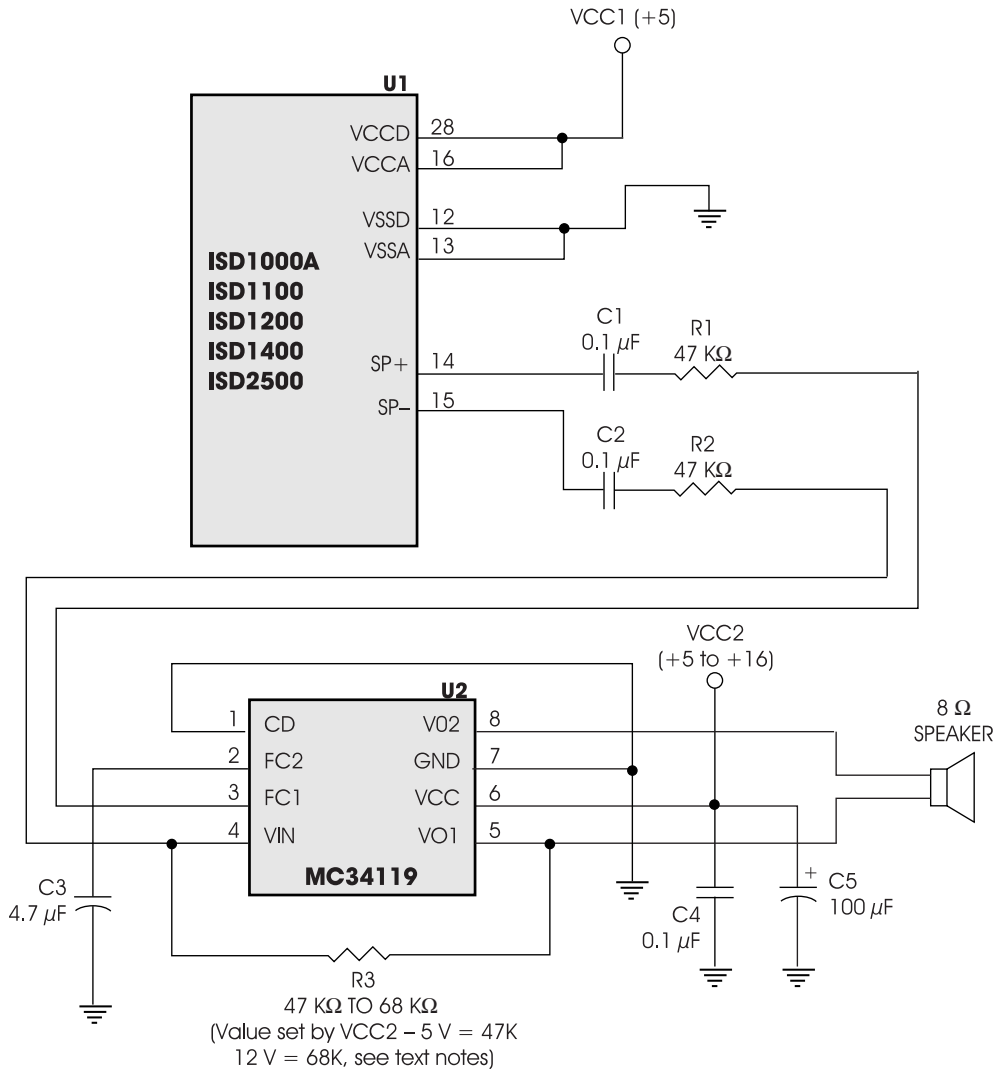


USING THE MOTOROLA MC34119 LOW-POWER AUDIO AMPLIFIER

The MC34119 low power audio amplifier integrated circuit, shown in Figure 2, was intended primarily for telephone applications. According to the Motorola data sheet, it operates over a voltage range from 2 to 16 volts and can supply up to 250 mW into a 32 Ω speaker. It can drive speaker loads down to 8 Ω. The MC34119 does not automatically power down. If the CD pin (pin 1) is taken to V_{CC}, however, the device will power down to typically less than 1/2 mA.

The circuit used with the MC34119 is similar to that used with the NSC device. The FC1 and VIN inputs are driven differentially from the ISD Speaker outputs. Speaker volume is set by adjusting the value of R3 which is a feedback resistor used to set gain in the MC34119. Care should be taken so that the Motorola amplifier's package power dissipation specification is not exceeded. The designer may wish to derive a control signal to drive the CD pin to lower circuit power consumption when not in use.

Figure 2: MC34119 Speaker Driver



WRITE ENDURANCE CONSIDERATIONS

Conventional EEPROM technology exhibits a long term failure mechanism defined by the term "Write Endurance." This means that each bit in the memory may be reliably erased and written only a certain number of times. Numbers commonly specified by EEPROM digital memory manufacturers for this phenomenon are 10^5 write cycles.

The ISD devices realistically exhibit a Write Endurance number of one to two orders of magnitude better than conventional EEPROM products for two reasons:

- The writing process used by ISD results in less stress on the memory cell. Digital EEPROMs program the cell with a large in-rush of current. This in effect "blasts" a "1" or "0" into the cell. The ISD devices meter small amounts of charge onto the cell during the closed loop writing sequence.
- A single cell failure during the programming of a digital EEPROM is devastating and renders the memory unusable. A single cell failure in a ISD device results in an imperceptible change in distortion. In fact, many random failures

would have to occur before recording quality would noticeably degrade.

ISD believes that typically 10^5 write cycles may be executed in an ISD device without noticeable effect on record and playback quality.

RECORDING TECHNIQUES

Some applications require the recording of sound from some other media into an ISD device. This is easily accomplished if care is observed in several areas:

Input levels

Care should be exercised during recording to ensure that the input level specifications are observed. If levels are too low, background noise may be objectionable. Too high a level during Record may cause clipping of the output waveform during playback.

ANA IN input

Driving the ANA IN input will result in the highest quality and lowest distortion recording. The effective dynamic range, however, will be less than when driving the MIC input because of the AGC in the microphone preamplifier. (50 mV P-P maximum to ANA IN.)

MIC input

Driving the MIC pin gives the largest dynamic range during record. However, this AGC controlled amplifier stage will contribute some distortion due to the gain control process. (20 mV p-p maximum to MIC.)

Program material

The user should experiment with the programming to be recorded. Certain types of music, speech, sounds, etc., may record better through one input than another. Also, program material with a large dynamic range may give unacceptable results because quiet passages may sound noisy while loud passages are distorted.

UNEXPECTED RECORD

Sometimes an unexpected recording takes place when a circuit is powered up. This "undesired recording" puts an EOM at the very beginning of the memory. Then, when one goes to playback the previously recorded message, it is gone! Actually, it is still there but the EOM is detected in the first row and the device quits playing. The original message is no longer accessible for normal playback from address 000.

The reason for this undesired effect is in the type of network used to control the $\overline{CE}$ pin. (The same effect can be observed on the ISD1100/1200/1400 $\overline{REC}$ pin.) Although the ISD device has a power down circuit so one does not need to disconnect the battery, some customers chose to disconnect the battery anyway. Depending upon their circuit design they may be able to eliminate all standby current this way. However, even when the power is normally connected all the time, the problem can appear when changing the battery.

This is because the V_{CC} voltage to the device may rise faster than the voltage at the control pins. The normal state of the control pins is HIGH. They are taken LOW to signal a request. They are normally held HIGH by external pull-up resistors. As long as power is applied, this is just fine. But, depending on the capacitance at the pin, and the value of the pull-up resistor, when the power is applied, the pin may go HIGH more slowly than the internal V_{CC}. So, after the device has sufficient V_{CC} to operate, 100 nanoseconds after the internal POR delay, it will detect a LOW at $\overline{CE}$. If P/$\overline{R}$ is also LOW, it will begin a Record Operation that will end very quickly as the time constant of the resistance and capacitance attached to the $\overline{CE}$ pin lets the voltage rise above the detection threshold.

A simple method to eliminate this situation is to have a capacitor (a starting value could be 0.001 μF) connected from the control pin to V_{CC}. Then, with power up, that capacitor will bring the pin voltage up with V_{CC} as it rises. This is because one cannot change the voltage across a capacitor instantaneously. Once the voltage is HIGH, the pull-up resistor will keep the pin HIGH until it is activated. Thus, the spurious Record command is eliminated.

It is important to note that this situation will not be noticed in all circuit designs, being dependent upon the capacitance of the printed circuit board and the device input itself. However, it should be accounted for to ensure the reliability of any design.

MESSAGE CONCATENATION

Prompting applications often need the concatenation of words or phrases to build sentences. This requires the ability to directly address a word or phrase, start the operation, then detect when the word has completed. This capability is included in all families of ISD Analog Storage Devices. The following example message demonstrates one method of achieving this goal.

Play the sentence "I like computers." An ISD2560 had been previously recorded with the following words, "I" located at address 95 (decimal), "like" located at address 140, and "computers" located at address 490.

The address of 95 (HEX 5F or 0101 1111) is placed on the ISD2560's address pins. A normal playback cycle is started by pulsing $\overline{CE}$ LOW. After the playback begins, $\overline{CE}$ remains HIGH. When playback ends, $\overline{EOM}$ will go LOW for 12.5 ms, then come back HIGH. Playback of the word "I" will not actually end until $\overline{EOM}$ goes back HIGH.

The address of 140 is now placed on the ISD2560's address inputs and another playback cycle is begun. The word "like" will now play and will not complete until the $\overline{EOM}$ signal pulses LOW, then goes back HIGH.

The address of 490 is now placed on the ISD2560's address inputs and a final playback cycle is begun. As with the other two steps, the word "computer" will not finish being played until $\overline{EOM}$ goes back HIGH.

CONCATENATION CONSIDERATIONS

There is an art to successfully creating good sounding concatenation. Timing, inflection, pitch and rhythm all work to help or hinder the finished "product" of words and phrases. The first step in successful concatenation is the preparation of a script of phrases and sentences to be recorded. From this script comes a list of needed words. It may be necessary to record and store some words more than once due to the required inflection in different phrases.

A master recording is made from this script. This recording is processed, if necessary, to eliminate unneeded pauses and noise. The master recording is then used to create a master chip with all the words and phrases at known addresses. Now we can say "I like computers" without anyone moving their lips.

CREATING A MASTER SOUND FILE

The following steps show one method of generating a master chip. A Creative Labs Sound Blaster 16™ is used with the ISD-SD101 Sound Development and Programming System.

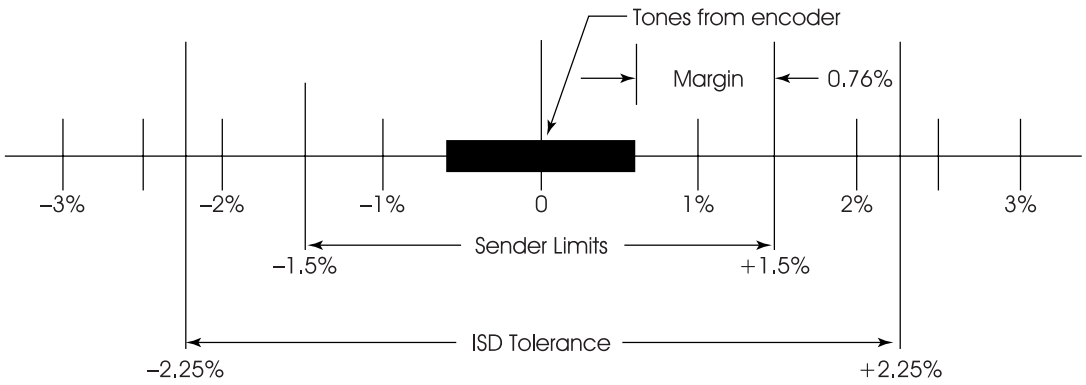
1. The list of words (with correct inflection indicated in some manner) is given to the announcer who makes an analog or digital recording of each one. This recording is loaded into the memory of an IBM® compatible PC using a Creative Labs Sound Blaster 16 operating under Windows™ versions 3.1 and 3.11. **The speech is stored in an 8-bit .wav file sampled at 22,050 Hz in the monophonic mode.**
2. The Creative WaveStudio™ program (or a similar sound editor) is used to edit each word from the list. Quiet periods, delays and noise may be edited out using this software. Record level may be changed and special effects added.
3. The editing software is used to generate one file per word or phrase in .wav format. These files are then converted to the .voc format.

4. The ISD-SD101 Sound Development and Programming System software is now loaded. The word and phrase .voc files are selected and brought into the program.
5. The graphical interface of the ISD-SD101 Software is used to position each sound file into the selected ISD device memory. Address boundaries, EOM locations and unused space are visually identifiable.
6. When required positioning and mapping of the sound files is achieved, the ISD-SD101 Software allows the generation of an address map of the sound files and creates a .chp file to be used to program one or more ISD devices.
7. The ISD-SD101 may be used to program up to eight devices at one time in a production environment.

SENDING & STORING DTMF WITH ISD DEVICES

Many people have asked about using the ISD devices to store and send DTMF dialing digits. This seems practicable since they are using the devices to store the message that will be sent when the telephone connection is made. By doing this they may eliminate an additional DTMF dialer chip in the product. The DTMF digits are "In-Band Signaling" as they are in the same frequency range as the voice passed through the telephone or radio network.

Figure 3: DTMF versus ISD Frequency Tolerance



Much of the time this idea will work well, especially if the voltage or temperature is not varied on the ISD device between record and playback. To be confident that this idea will always work, the ISD devices must be clocked from external clock sources with a tolerance of less than ±0.25 percent (refer to Figure 3).

This is because of the following facts:

- The Bell Telephone DTMF sending tolerance is ±1.5 percent of the nominal values.
- DTMF encoder chips are crystal controlled but, because of their divider chains, are actually creating tones that are +0.74/–0.54 percent, for example, when the crystal is exactly 3.579545 MHz.
- The internal oscillator specification for most ISD devices is ±2.25 percent over voltage and temperature.

Dividing the margin in half to allow for the worst case variation between Record and Play Modes gives 0.38 percent. This suggests a tolerance of better than ±0.25 percent is needed on the external clock signal provided to pin 26 of the ISD devices. It can be either TTL or CMOS levels. Using the ISD2560 as an example, the internal clock frequency is 1.024 MHz for the 8 KHz sampling rate.

In a typical application that utilizes a microprocessor or microcontroller there is a crystal oscillator to provide the system clock. This is often 2, 4, or 8 MHz. By using the necessary divider stages a 1 MHz signal could be made available to the ISD2560. This is close enough to 1.024 MHz to use without any problem. The requirement is not so much exact frequency as it is constant or repeatable frequency. The main system crystal can provide that.

OPERATION ABOVE 5.5 VOLTS

The standard operational voltage specification for packaged ISD products (except the ISD2500 series) is 4.5 to 5.5 volts. Above 5.5 volts, distortion may increase unless care is taken to make sure the internal storage array is not overdriven. ISD recommends that a resistor of 5.1 KΩ be put in series with the capacitor between ANA IN and ANA OUT. An example of this network may be found between pins 20 and 21 in "Circuit Examples" under Application Information.